REMARKS

Claims 1-22, 24-30, 32-38 and 40-68 are pending in the application, with claims 1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61 and 65 being independent. Claims 23, 31 and 39 have been canceled and claims 1-3, 5-7, 10, 11, 14, 15, 17-19, 21, 22, 25-27, 29, 30, 33-35, 37, 38, 41-43, 46, 47, 49-51, 54, 58, 59, 62, 63 and 65-67 have been amended. No new matter has been added.

Initially, applicant acknowledges with appreciation the Examiner's allowance of claims 9, 10, 12-14, 16, 45, 46, 48, 53, 54, 56-58, 60-62 and 64.

Claims 3, 7, 11, 15, 19, 27, 35, 43, 47, 51, 55, 59, 63 and 67 have been amended in response to the rejection under section 112, first paragraph. As amended, the claims recite that the capacitance wiring line and the pixel electrode are formed from the same conductive film. This recitation finds support, for example, at page 8, lines 14-15 of the application. In view of the amendments, applicant requests reconsideration and withdrawal of this rejection.

Claims 3 and 7 have been amended to recite "a pixel electrode" in response to the rejection under section 112, second paragraph. In view of the amendments, applicant requests reconsideration and withdrawal of this rejection.

Claims 1, 4, 5, 8, 17, 20, 21, 24, 25, 28, 29 and 32 have been rejected as being anticipated by Kimura. Applicant requests reconsideration and withdrawal of this rejection for the reasons discussed below.

Each of independent claims 1, 5, 17 and 25 has been amended to recite a thin film transistor over a substrate; an interlayer insulating film over the thin film transistor; and a capacitor storage over the insulating film, the capacitor storage having a connection wiring line, a capacitance wiring line and an insulating film between the connection wiring line and the capacitance wiring line, such that the capacitance wiring line is formed over an interlayer insulating film over a thin film transistor. Kimura does not disclose this feature. Instead, as illustrated by Figs. 6(a) and 6(b) of Kimura, a capacitance wiring line 113 of Kimura is formed on a gate insulating film of a thin film transistor, not over an interlayer insulating film formed

over a thin film transistor. Applicant requests reconsideration and withdrawal of the rejection of claims 1, 5, 17 and 25, and the claims depending from them, for at least this reason.

Amended claims 21 and 29 recite a first capacitor storage and a second capacitor storage over the first capacitor storage. The first capacitor storage has a capacitance electrode, a semiconductor layer, and a first insulating film formed between the capacitance electrode and the semiconductor layer, and the second capacitor storage has the capacitance electrode, a power supply line, and a second insulating film formed between the capacitance electrode and the power supply line. The capacitance electrode is formed of a same conductive film as a gate electrode of a thin film transistor. Kimura do not describe or suggest two capacitor storages arranged in the manner recited in claims 21 and 29. Accordingly, applicant requests reconsideration and withdrawal of the rejection of claims 1, 5, 17 and 25, and the claims depending from them, for at least this reason.

Claims 65 and 68 have been rejected as being anticipated by Murade. As amended, independent claim 65 recites, among other elements, forming a capacitance wiring line on a different layer from a gate electrode of a thin film transistor. Murade does not describe or suggest such an arrangement. Rather, Murade describes a layer 1f that is a semiconductor layer and a layer 3b that is a conductive layer formed on a same layer as a gate electrode. Accordingly, applicant requests reconsideration and withdrawal of the rejection of claims 65 and 68 for at least this reason.

Claims 41 44, 49 and 52 have been rejected as being obvious over Kimura in view of Murade. Claims 41 and 49 have been amended to recite, among other elements, thin film transistors over a substrate; an interlayer insulating film over the thin film transistors; and a capacitor storage over the insulating film, with the capacitor storage having a connection wiring line, a capacitance wiring line and an insulating film between the connection wiring line and the capacitance wiring line, such that the capacitance wiring line is formed over an interlayer insulating film over thin film transistors. As discussed above with respect to claim 1, Kimura does not describe or suggest this feature. Nor does Murade remedy this failure of Kimura.

Accordingly, for at least this reason, applicant requests reconsideration and withdrawal of the rejection of claims 41 and 49, and the claims depending from them.

Claims 33, 36, 37 and 40 have been rejected as being obvious over Kimura in view of Blalock.

Claim 33 has been amended to recite, among other features, thin film transistors over a substrate; an interlayer insulating film over the thin film transistors; and a capacitor storage over the insulating film, with the capacitor storage having a connection wiring line, a capacitance wiring line and an insulating film between the connection wiring line and the capacitance wiring line such that the capacitance wiring line is formed over an interlayer insulating film over thin film transistors. As discussed above with respect to claim 1, Kimura does not describe or suggest this feature. Nor does Blalock remedy this failure of Kimura. Accordingly, for at least this reason, applicant requests reconsideration and withdrawal of the rejection of claims 33 and 36.

Claim 37 has been amended to recite, among other features, a first capacitor storage having a capacitance electrode, a semiconductor layer, and a first insulating film formed between the capacitance electrode and the semiconductor layer, and a second capacitor storage having the capacitance electrode, a power supply line, and a second insulating film formed between the capacitance electrode and the power supply line, with the capacitance electrode being formed of a same conductive film as a gate electrode of a thin film transistor. Neither Kimura, Blalock, nor any combination of the two describes or suggests two capacitor storages arranged in the manner recited in claim 37. Accordingly, for at least this reason, applicant requests reconsideration and withdrawal of the rejection of claims 37 and 40.

Claims 2, 6, 18, 22, 26 and 30 have been rejected as being obvious over Kimura in view of Suzawa, claims 34 and 38 have been rejected as being obvious over Kimura in view of Blalock and Suzawa, claims 42 and 50 have been rejected as being obvious over Kimura in view of Murade and Suzawa, and claim 66 has been rejected as being obvious over Murade in view of Suzawa. Applicant requests reconsideration and withdrawal of these rejections because Suzawa

does not remedy the failure of the other references to describe or suggest the subject matter of the independent claims from which these claims depend.

For the reasons provided above, applicant submits that all claims are in condition for allowance.

A check in the amount of $410.00 is enclosed for the Petition for Extension of Time fee. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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